SHARP SERVICE MANUAL

The photo shows Model ER-1920.

CODE : 00ZER2395SMHE

ELECTRONIC CASH REGISTER

SECTION 2 HARDWARE

MODEL ER-1910/1920 ER-2385/2395

ER-1910/1920 (Europe Version)
ER-2385/2395 (U.S.A., Canada, South Africa Version)

The photo shows Model ER-2395.

CONTENTS

Note: The service manual of the above models is consisted of four major manuals as follows. Therefore, please refer to other manuals together with this service manuals in your service.

1-1. Section 1 programming manuals for U.S.A., Canada, South Africa, etc. 00ZER2395SMBE
1-2. Section 1 Basic manuals for Europe, etc. 00ZER1920SMBE
2. Section 2 Hardware description for all countries (except Japan) 00ZER2395SMHE
3. Circuit diagram and PWB layout for all countries 00ZER2395CD1M
4. Printer manual for all countries 00ZCR802ASM/M

Note: Europe Version = U.K., W. Germany, Australia and others.

SHARP CORPORATION

1. Reference Documents

Manual name	Contents	Manual code	New mark	Applicable area and models: Europe Version (U.K., Germany, Australia and others) ER-1910	ER-1920	U.S.A version (U.S.A., Canada, South Africa and others) ER-2385	ER-2395
1) Section 1 Basic manual	Specification, SRV Programming, option etc.	00ZER1920SMBE	N	○			
Section 1 Prog. manual		00ZER2395SMBE	N			○	
2) Section 2 Hardware	Circuit description. Dig., Service option etc.	00ZER2395SMHE	N	○		○	
3) Circuit diagram and PWB layout	Main board, key board etc.	00ZER2395CD1M	N	○		○	
4) Printer manual	CR-802, 812, 911A	00ZCR802SM//E		○		○	
	CR-802A, 812A	00ZCR802ASM/M	N	○	○	○	
	CR-911D	00ZCR911DSM/M	N				○
5) Cash register basic manual	Basic circuit descripiton	—		○		○	
6) Operation manual	PGM programming, Registration etc.	TINSE7009RCZZ	N			○ (U.S.A.)	
		TINSM7012RCZZ	N	○			
		TINSK7047RCZZ	N			○ (Except U.S.A.)	

2. Block Diagram

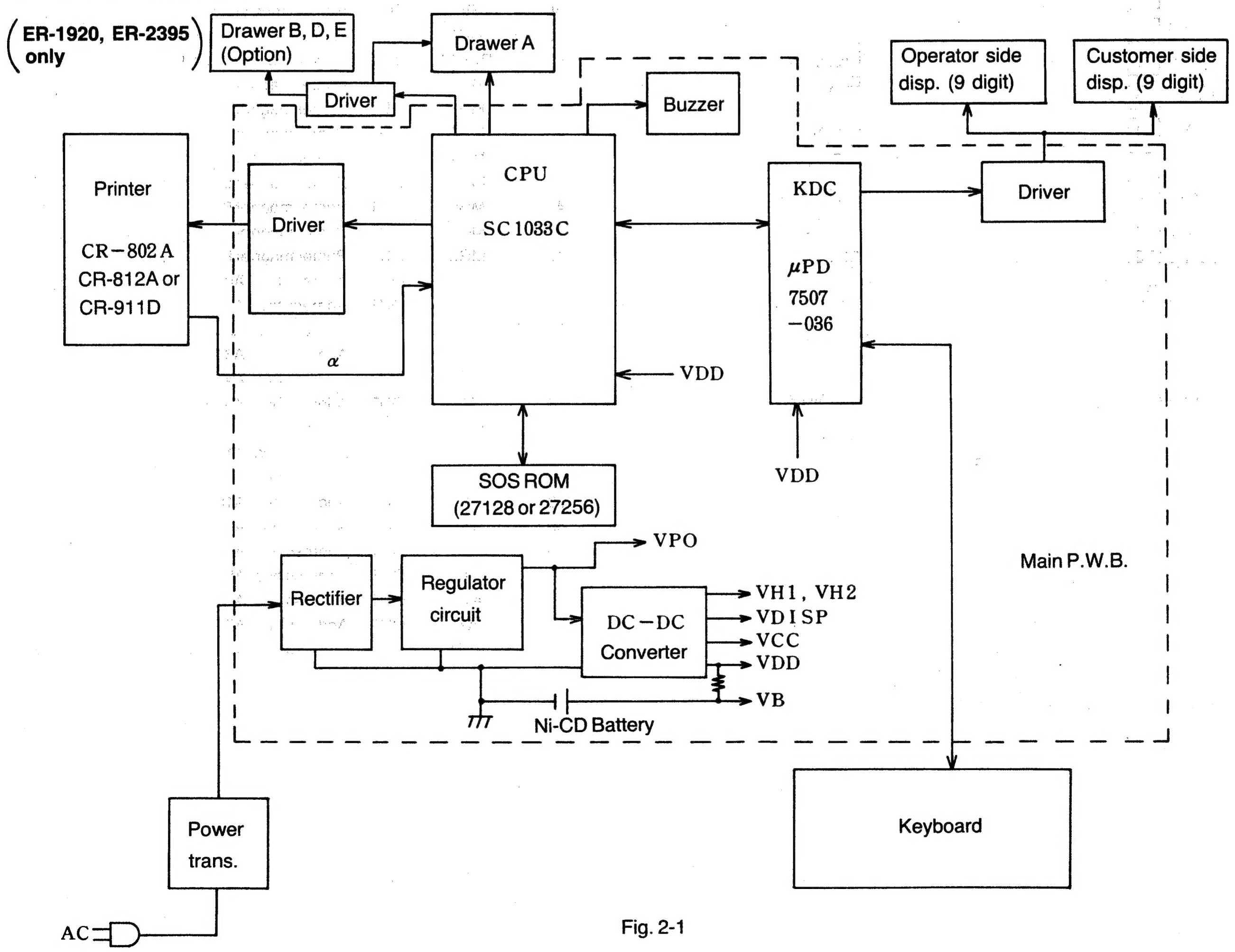


Fig. 2-1

3. CPU pin description

3-1. CPU (SC1033C)

The SC1033C is a single chip microprocessor which has an internal ROM, RAM, and serial I/O.

Pin configuration

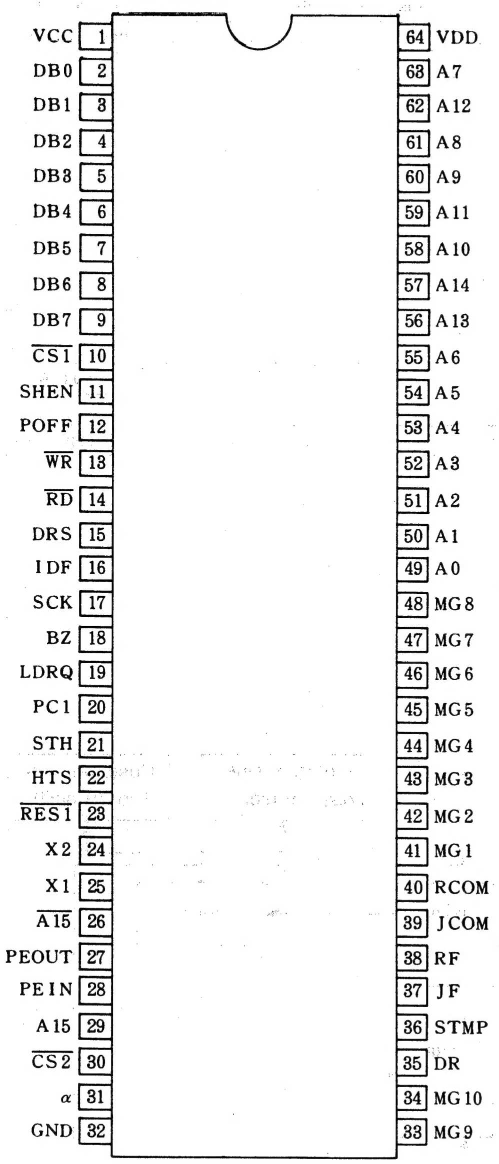


Fig. 3-1

3-2. Signal description

Pin No.	Signal name	I/O	Description
1	Vcc	—	+5V
2 9	DB0 ~ DB7	I/O I/O	Data bus line
10	$\overline{CS1}$	IN	Chip select 1 (connected with $\overline{A15}$)
11	SHEN	IN	Shift enable
12	POFF	OUT	Not used
13	$\overline{WR}$	OUT	Write signal (normally not used)
14	$\overline{RD}$	OUT	Read signal
15	DRS	IN	Drawer open sensor line (not used)
16	IDF	OUT	Printer motor drive signal
17	SCK	OUT	Shift clock (KDC)
18	BZ	OUT	Buzzer signal
19	LDRQ	OUT	Load request (KDC)
20	PC1	IN	Not used (LSI test pin, normally connected to GND)
21	STH	IN	8-bit serial input (KDC)
22	HTS	OUT	8-bit serial output (KDC)
23	$\overline{RES1}$	IN	Reset input
24	X2	—	3MHz oscillator
25	X1	—	3MHz oscillator
26	$\overline{A15}$	OUT	Address bus, $\overline{A15}$
27	PEOUT	OUT	PE signal output
28	PEIN	IN	PE signal input
29	A15	OUT	Address bus, A15
30	$\overline{CS2}$	OUT	Chip select 2 (normally not used) SOS ROM
31	α	IN	α signal
32	GND	—	GND
33	MG9	OUT	Printer magnet 9
34	MG10	OUT	Printer magnet 10
35	DR	OUT	Drawer open signal
36	STMP	OUT	Stamp signal
37	JF1	OUT	Journal feed signal
38	RF	OUT	Receipt feed signal
39	JCOM	OUT	Journal common signal
40	RCOM	OUT	Receipt common signal
41	MG1	OUT	Printer magnet 1
42	MG2	OUT	Printer magnet 2
43	MG3	OUT	Printer magnet 3
44	MG4	OUT	Printer magnet 4
45	MG5	OUT	Printer magnet 5
46	MG6	OUT	Printer magnet 6
47	MG7	OUT	Printer magnet 7
48	MG8	OUT	Printer magnet 8
49	A0	OUT	Address bus, A0
50	A1	OUT	Address bus, A1
51	A2	OUT	Address bus, A2
52	A3	OUT	Address bus, A3
53	A4	OUT	Address bus, A4
54	A5	OUT	Address bus, A5
55	A6	OUT	Address bus, A6
56	A13	OUT	Address bus, A13
57	A14	OUT	Address bus, A14
58	A10	OUT	Address bus, A10
59	A11	OUT	Address bus, A11
60	A9	OUT	Address bus, A9
61	A8	OUT	Address bus, A8
62	A12	OUT	Address bus, A12
63	A7	OUT	Address bus, A7
64	VDD	—	VDD (rechargeable battery voltage during power down)

3-3. KDC (μPD7507-036)

The μPD7507-036 is called KDC (Key Display Controller) which is used to control the keyboard, display, and clock. Communication is performed with the SC1033C CPU via the 8-bit serial interface.

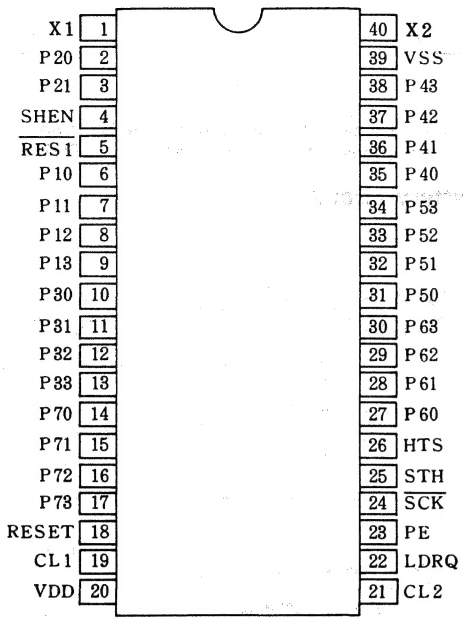
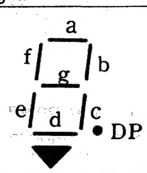


Fig. 3-2

3-4. Signal description

Pin No.	Signal name	I/O	Description
1	X2	—	Timer clock
2	P20	OUT	Key scan signal
3	P21	OUT	Display drive signal 9/key scan signal
4	SHEN	OUT	Shift enable
5	$\overline{\text{RES1}}$	OUT	Reset signal
6	P10	IN	Key return signal
7	P11	IN	Key return signal
8	P12	IN	Key return signal
9	P13	IN	Key return signal
10	P30	OUT	Display drive signal 1/key scan signal
11	P31	OUT	Display drive signal 2/key scan signal
12	P32	OUT	Display drive signal 3/key scan signal
13	P33	OUT	Display drive signal 4/key scan signal
14	P70	OUT	Display drive signal 5/key scan signal
15	P71	OUT	Display drive signal 6/key scan signal
16	P72	OUT	Display drive signal 7/key scan signal
17	P73	OUT	Display drive signal 8/key scan signal
18	RESET	INT	Reset input
19	CL1	—	Basic clock
20	VDD	—	VDD (rechargeable battery voltage during power down)
21	CL2	—	Basic clock
22	LDRQ	IN	Load request
23	PE	IN	PE
24	$\overline{\text{SCK}}$	IN	Shift clock
25	STH	OUT	Serial output data
26	HTS	IN	Serial input data
27	P60	IN	Key return signal
28	P61	IN	Receipt/journal key return signal
29	P62	IN	Mode switch return signal
30	P63	OUT	Display drive ▼
31	P50	OUT	Display drive g
32	P51	OUT	Display drive f
33	P52	OUT	Display drive e
34	P53	OUT	Display drive d
35	P40	OUT	Display drive c
36	P41	OUT	Display drive b
37	P42	OUT	Display drive a
38	P43	OUT	Display drive DP
39	Vss	—	GND
40	X1	—	Timer clock



4. Circuit description

4-1. Oscillation circuit

(1) CPU clock

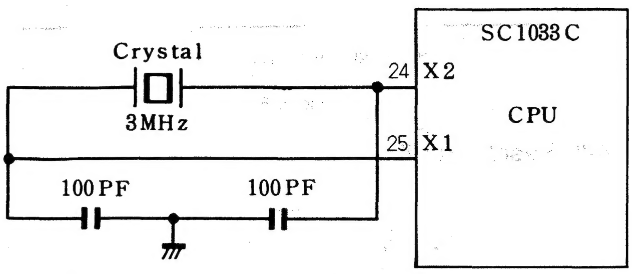


Fig. 4-1

The basic clock is created in the 3MHz crystal oscillator and connected directly with the CPU. The following shows the waveforms of signals, X1 and X2.

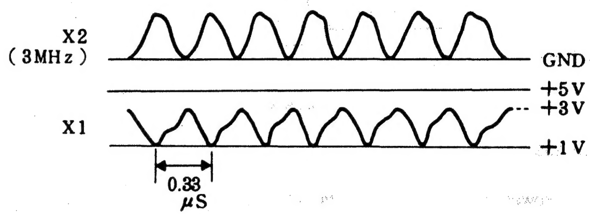


Fig. 4-2

(2) KDC (Key Display Controller) clock

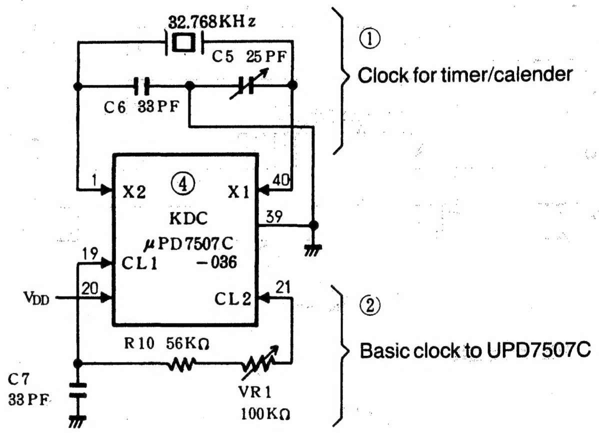


Fig. 4-3

From this circuit is delivered the timer, calendar, and μPD7505C basic clock.

1) Timer and calendar clock
   Clock frequency generated across X1 and X2 is adjusted by the trimmer capacitor (C5) and supplied to the KDC. The trimmer capacitor has been factory adjusted using the error meter, it should never be readjusted.
2) μPD7507C basic clock
   Clock frequency coming across CL1 and CL2 is adjusted by the potentiometer (VR1) and supplied to the KDC.
   Even if this frequency is observed on the oscilloscope, it would not be possible to see an exact waveform because of a capacitance in the probe.
   So, one of the following two methods may be used.

[Adjustment-1]

Observe on the oscilloscope the waveform on the test pin 1 (pin 3) of the μPD7505C and adjust it using VR so that the following waveform can be seen.

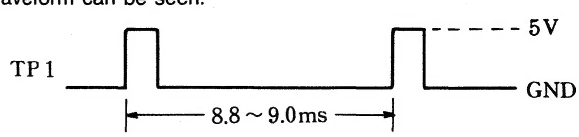


Fig. 4-4

[Adjustment-2]
Execute Job #15 in the SRV mode and adjust VR so that the waveform on TP1 should be as shown below.

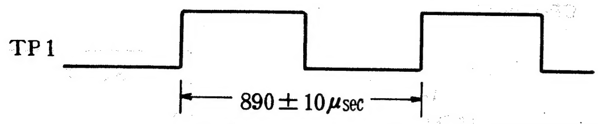


Fig. 4-5

4-2. Reset circuit

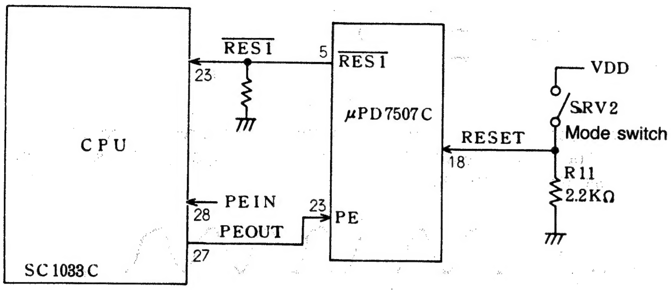


Fig. 4-6

Timings

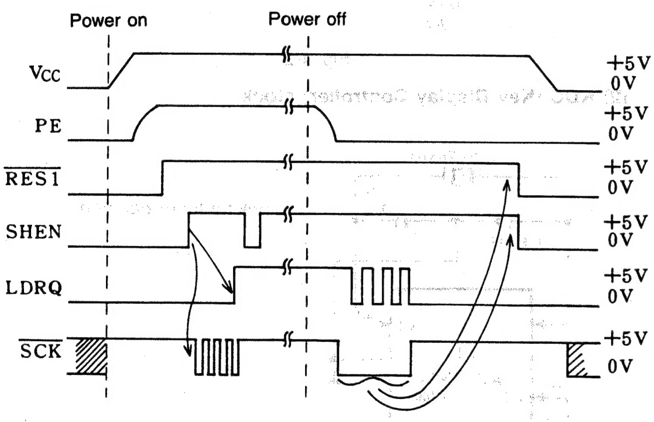


Fig. 4-7

4-3. PE circuit

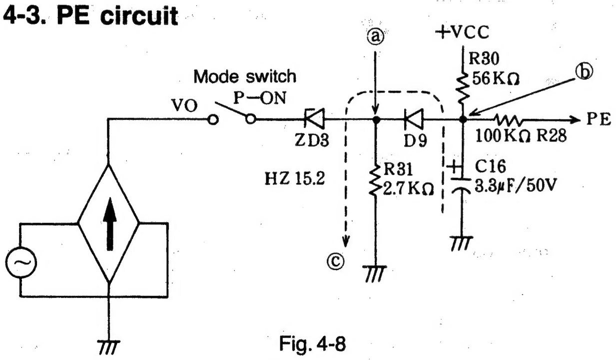


Fig. 4-8

When the mode switch is set to any position other than OFF, the switch shown in the figure above turns on. (VO connected with P-ON.) ⓐ becomes about 18V via ZD3. As the power is turned on, VCC generated in the DC-DC converter turns to 5V. Voltage at point ⓑ of C16 gradually increases by VCC. When VO disengages from P-ON inside the (PE) mode switch, the charge in C16 is discharged to the direction shown with ⓒ because the voltage at point ⓐ becomes null. So, the voltage at point ⓑ drops down to GND level.

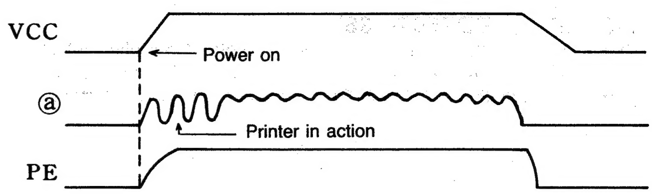


Fig. 4-9

The PE signal is waveform shaved within the SC1033C through the NOT gate and supplied to the CPU and KDC (μPD7507).

4-4. Battery circuit

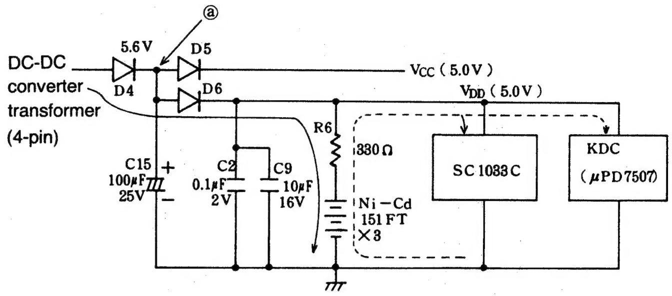


Fig. 4-10

⟶ : Battery recharge current

- - - -> : Battery discharge current

Voltage at each point is as follows:

AC supply	Point ⓐ	V_{DD}
OFF	0V	+3.6V
ON	+5.6V	+5V

4-5. Communication between the CPU and the KDC (μPD7507C)

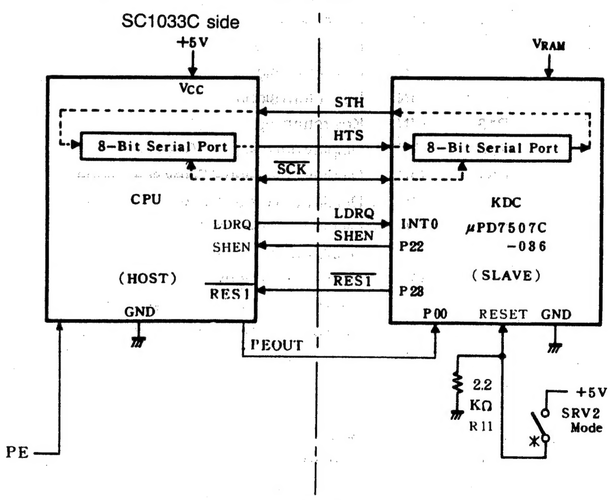


Fig. 4-11

STH	:	Serial input
HTS	:	Serial output
SCK	:	Shift clock
LDRQ	:	Load request
SHEN	:	Shift enable
RES1	:	System reset
PE	:	Power down detection
RESET	:	KDC reset

(1) During power off
Power is supplied to the KDC even if the power is off. During this period, the KDC performs the following operations.
(KDC operating voltage is +3V to +7V)
1) Keeping time for the timer and calendar.
2) Detection of the PE signal level...The KDC checks the POF signal at 500msec.*

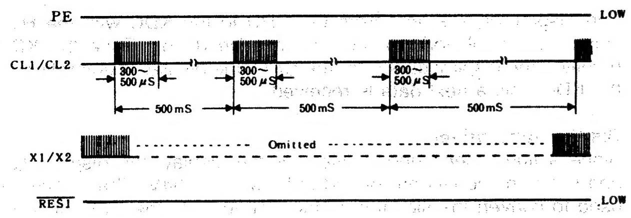


Fig. 4-12

The CPU (SC1033C) is not operating as +5V is not in supply during power off.

(2) When power is turned on
When the power is turned on, PE is forced high and sent to the KDC. The KDC having received a high state of PE, the KDC issues RES1 to reset the CPU.

(3) When power is turned off
When the power is turned off, PE is forced low and directly sent to the CPU. After the CPU finishes executing the required processing, it sends LDRQ and SCK to the KDC requesting to send RES1. The CPU thus received RES1 is then reset.

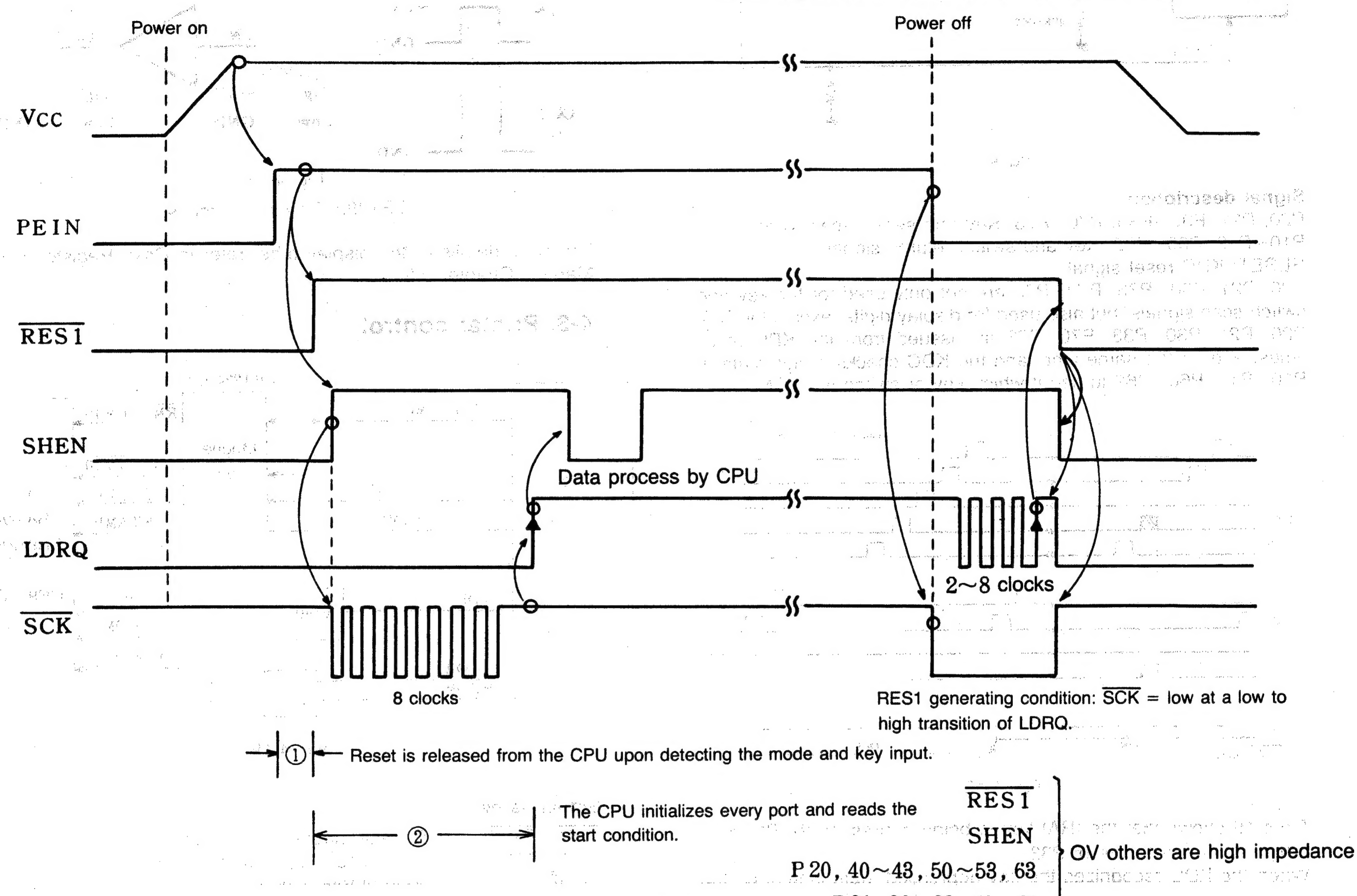


Fig. 4-13

(4) KDC reset
When the mode switch is turned on in the SRV2 mode, RESET is forced high (5V) and the KDC is reset. RES1 is pulled down with a 12KΩ resistor, the CPU is reset by the RES1. When it is changed from the SRV2 to SRV1 mode, RESET is forced low and the KDC is released from the reset. Then, the KDC turns RES1 high to release the CPU from the reset.

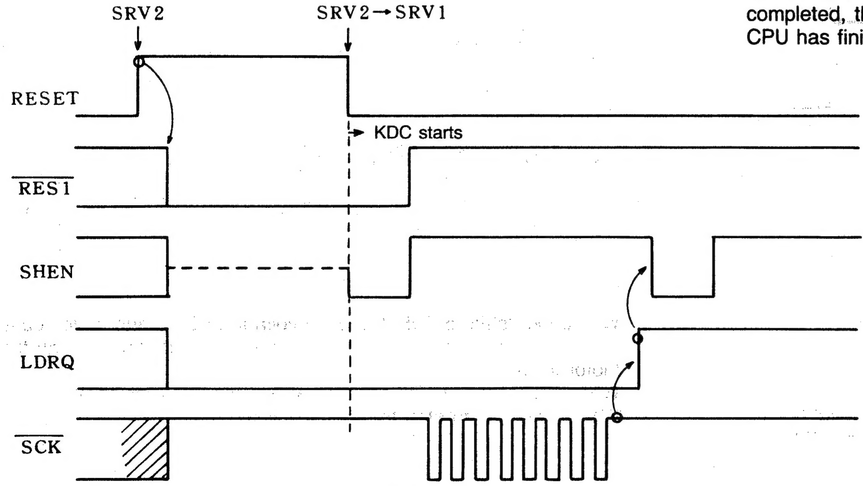


Fig. 4-14

(5) Data transfer between the CPU and the KDC
Data is transferred through the CPU and KDC 8-bit serial port in synchronization with SCK received from the CPU.
To transfer data from the CPU to the KDC, the STH line is used.
To transfer data from the KDC to the CPU, the HTS line is used.
Data transfer can take place with a SHEN which is an output from the KDC. When the CPU senses a high state of SHEN, it responds with SCK to carry out data transfer. When data transfer has been completed, the CPU sends a LDRQ to the KDC to inform that the CPU has finished receiving and sending.

4-6. Key and switch read

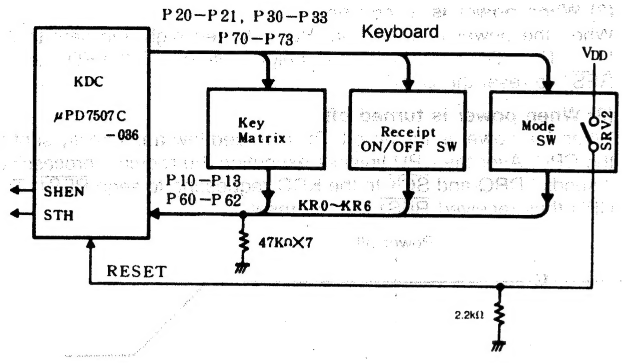


Fig. 4-15

Signal description
P20, P21, P30~P33, P70~P73: Key and switch scan signal
P10~P13, P60~P62: Key and switch returns signal
RESET: KDC reset signal
P20, P21, P30~P33, P70~P73 are not only used for the key and switch scan signals, but also used for display digits, except for P20.
P20, P21, P30~P33, P70~P73 are issued from the KDC at all times, and, at the same time, and the KDC checks a high state of P10~P13, P60~P62 to see if which key or switch is at ON.

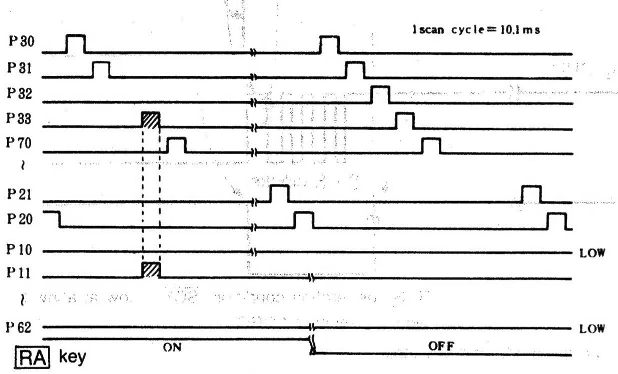
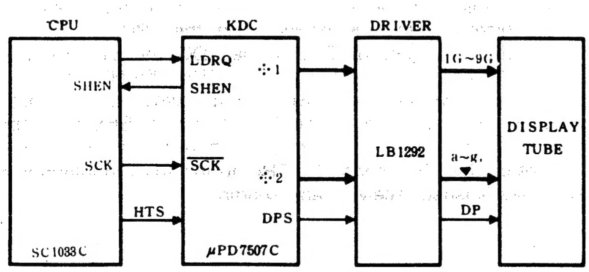


Fig. 4-16

Fig.4-16 shows that the [RA] key is being depressed for P11 is at a high level in the time of P33.
When the KDC recognizes the key depressed, data is sent on the STH line in response to the request from the CPU.

4-7. Display control



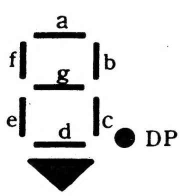


Fig. 4-17

Signal description
*1: P20, P30~P33, P70~P73(1G~9G): Display digit signal
*2: P43~P40, P53~P50, P63(a~g, ▼, DP): Display segment signal
P43 (DP): Decimal point

The display data is sent from the CPU to the KDC with the HTS signal and displayed via the display tube driver. Once the KDC received the display data from the CPU, the display is controlled by the KDC until a next data is received.

Display tube driver
Since a fluorescent tube is used for the display, the display digit and segment signals are operated by about +34V. The LB1292 is used to convert the signal from the TTL level to the +34V level.

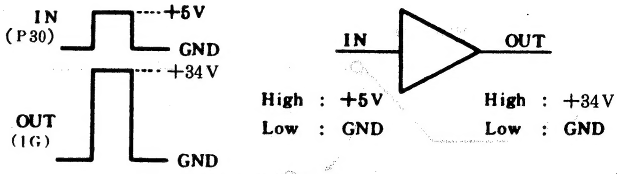


Fig. 4-18
LB1292: Driver×6 circuits

For more details of the display tube, refer to Cash Register Basic Manual, Chapter 9-3.

4-8. Printer control

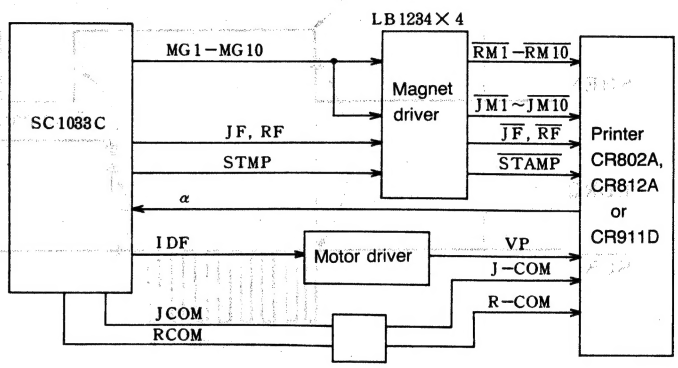


Fig. 4-19

Signal name

RM1~RM10	:	Receipt magnet select signal
JM1~JM10	:	Recording magnet select signal
JF-JF	:	Journal feed signal
RF-RF	:	Receipt feed signal
STMP-STAMP	:	Stamp signal
α	:	Printer interface signal
IDF	:	Motor drive signal
JCOM	:	Journal common signal
RCOM	:	Receipt common signal

For detail of printer, refer to CR802A, CR812A, CR911D, CR-802, CR-812, and CR-911A Printer Manual.

Motor drive circuit

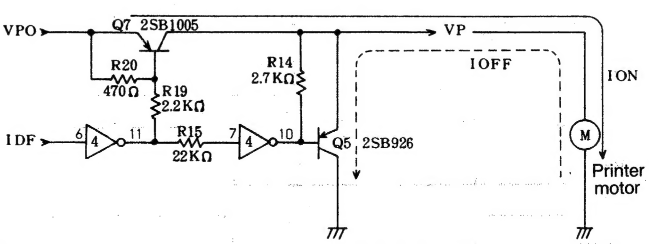


Fig. 4-20

With a high state of IDF, the base voltage of Q7 starts to decrease via IC4 and Q7 goes active which causes ION to flow through the motor to run it.
When IDF goes low, Q7 comes inactive and Q5 turns on. With this, IOFF is applied to stop the motor quickly.

4-9. Drawer control

[Without option drawer]

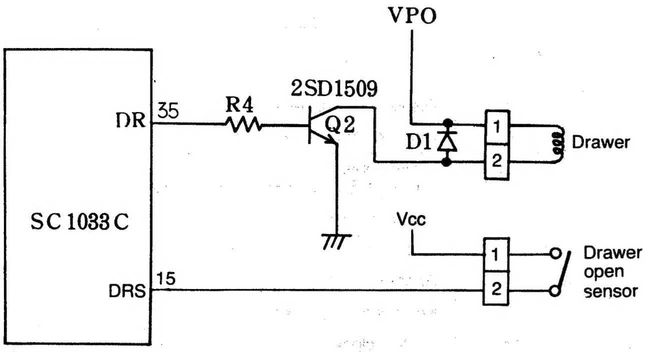


Fig. 4-21

The DR signal output from the pin 35 of the SC1033 drives Q2 to apply current to the drawer magnet. D1 is used to prevent a counter-electromotive force.

[With option drawers]

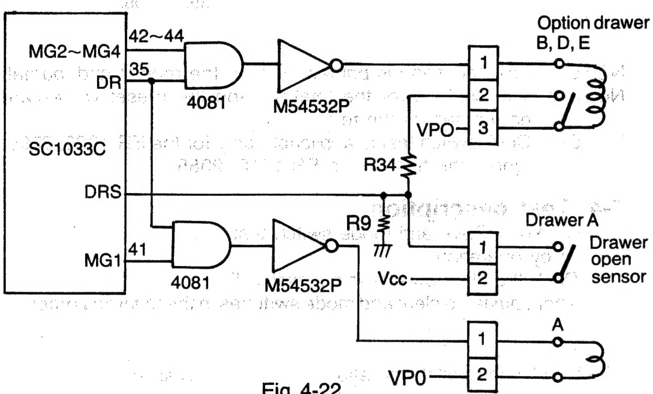


Fig. 4-22

In case an optional drawer is in use, drawers are driven by the DR signal issued from the pin 35 of the SC1033C and MG1 through MG4. A spark killer diode is contained in the M54532P.

4-10. Power supply circuit

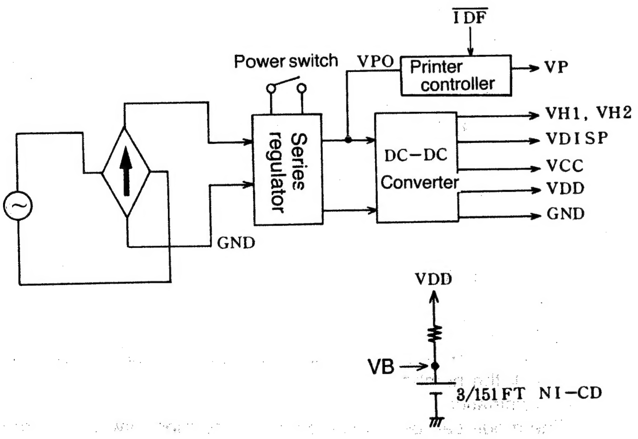


Fig. 4-23

VPO	:	Drawer +17.6V~-19.5V
VP	:	Printer +18V
VH1, VH2	:	Display heater +3.5V (rms)
VDISP	:	Display tube plate and grid +34V (+28.8V~+37.4V)
VCC	:	Circuit drive +5V (+4.5V~+5.5V)
VB	:	Power off time CPU & KDC drive +3.6V, min.
VDD	:	Power supply to CPU and KDC +5V (+4,5V~+5.5V)

VPO circuit

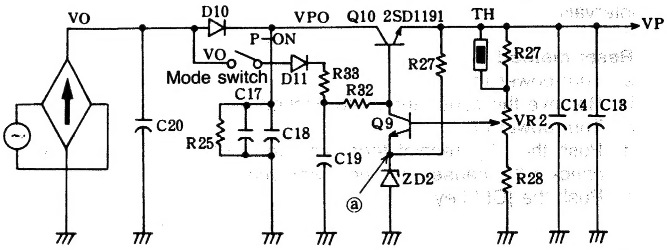


Fig. 4-24

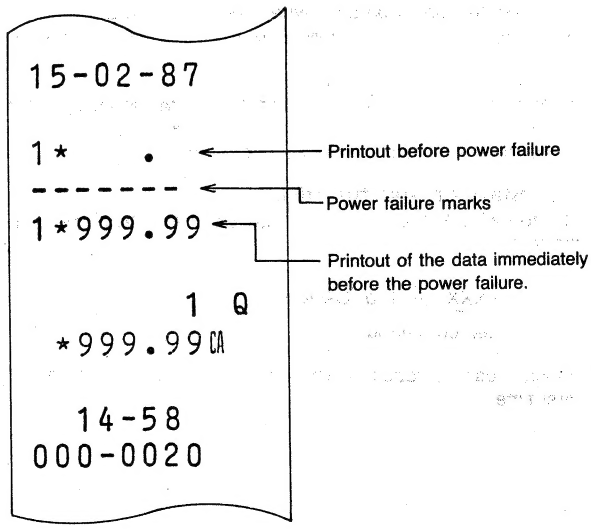
1) The base voltage is not applied to Q10 when V0 is not shorted with P-ON within the mode switch (power off), Q10 is at the OFF state.
2) When V0 is shorted with P-ON, base voltage is added to Q10 so that it goes active.
3) With an active state of Q10, the voltage VP0 starts to rise.
4) When the voltage at point ⓐ reaches 10V via R27, ZD2 then comes active.
5) If the base voltage is added to Q9 in this moment, Q9 is turned on and Q10 turns off.
6) As Q10 turns off, VP0 then starts to drop.
7) As VP0 starts dropping, it also causes Q9 base voltage to decrease and Q9 turns off finally.
8) Q10 starts to rise again and VP0 begins to rise.
9) VP0 is controlled stable by repeating the above steps, 5) thru 8).

5. Power failure/motor lock mechanical action and measures

5-1. Action at power failure (power off)

When the power is turned off in a middle of printing operation due to a power failure, the CPU executes the power failure process.

(1) When a power failure is encountered during printing operation, power failure marks (.....) are printed on a next line upon the recovery of power, and the printout lost at the time of power failure is correctly produced on a next line.
(2) If power failure was met other than during printing operation, the operation resumes in succession to the operation suspended at the time of power failure, when the power supply is recovered.



5-2. Action at the time of a printer motor lock-up

When the motor stops rotating due to a paper misfeed, etc., the power supplied to the motor is suspended to prevent the motor coil from burning out. An intermittent beeping will occur at one second intervals.

Reset method

a. Turn power off.
b. Remove the cause the motor locked.
c. Turn power on.
d. Push the [↑] (receipt feed) key and [↑] (journal feed) key to check if the cause has been removed.
e. Push the [CL] key.

6. Adjustments

6-1. Clock adjustment

VR1 (100KΩ), TP1⟷GND
Refer to Paragraph 4-1.

6-2. Error adjustment

Trimmer capacitor C5, TP1⟷GND
Since it has been factory adjusted, no adjustment should be made.

6-3. Printer speed adjustment

VR2 (6.8KΩ), TP2⟷GND

VR2 adjustment

The Q9 base voltage can be changed using VR2 to adjust printer speed.

1) Apply the oscilloscope probes across GND and the test pin TP2.
2) Do master reset and feed journal paper continuously.
3) Observe the waveform on the oscilloscope and adjust it as shown below.

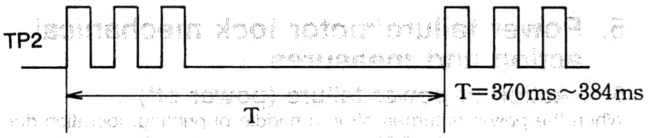


Fig. 4-25

7. Test functions (ER-1910/1920/2385/2395)

7-1. Prerequisite

This test function operates when the test program stored in the SC1003C CPU internal ROM. The following are required in order to execute the function.

a. The power supply to the logic circuit must be normal.
b. Both the CPU input pins and CPU internal logic circuits are functioning normally and that the entire KDC (μPD7507), and its address and data buses are operating normally.

7-2. Start of test function

The following key operation is required in the SRV1 mode to start the test.

XXXX → [TL] or [CA/AT]
Test command

Master reset is required when the system is to be started for the first time.

7-3. List of test commands

Test No.	Test command	Test description
1	1	Clerk/Mode switch test
2	XXXX02 *1	Keyboard test
3	3	Display and buzzer test
4	4	Receipt ON/OFF switch test
5	5, 6, 7, 8	Drawer open test (The code 6 to 8 are for optional drawers)
6	9	Continious print tes
7	10, 11, 12	ROM test
8	13	RAM test
9	14	Key position code test
10	15	System clock test
11	16	Counter clock test
12	XXXX00 *1	Sequential test – 1
13	XXXX22 *1	Sequential test – 2 (drawer open sensor disregarded)
Note: *1 XXXX:	Sum check data for standard key layout	ER-1910→ 548 ER-1920→ 916 ER-2385→ 815 ER-2395→ 1062

NOTE-1: Test message is printed on both the receipt and journal.
NOTE-2: The contents of the totalizer and the preset values are not erased by the test.
NOTE-3: Clerk switch test is applicable only for the ER-1920, 2395. Ignore the test for the ER-1910, 2385.

7-4. Test description

1) Test No.1: Clerk and mode switch test
① Key operation
Push the clerk switch→clerk switch E.
Then, push the clerk and mode switches in the following order.

Clerk and mode switch operation	Display	
Clerk SW. A	With clerk switch model only. If not, skip this part.	01
Clerk SW. B		02
Clerk SW. D		04
Clerk SW. E		08
Mode SW PGM		01
[∽] or VOID		02
⏻ or OFF		
OPX/Z or TIME		03
REG		04
X1		05
Z1		06
X2/Z2		07
SRV1		0.00

② Description
As the clerk and mode switch position number is displayed, check the number.
③ Termination
The mode can be terminated when the mode switch is turned to the SRV1 side from other position.
Termination print at error -------01E

Termination print at normal end 01

NOTE:Though the display may sway during this test, it is not a malfunction.

2) Test No.2: Keyboard

① Key operation

$\underbrace{\times\ \times\ \times\ \times}_{\text{Sum check data}}$ $\underbrace{0\ 2}_{\text{Test command}}$ → TL or CA/AT

(1) Enter the test command in succession to the sum check data of the model.

Key operation	Display
ER-1910→ 548	54802
ER-1920→ 916	91602
ER-2385→ 815	81502
ER-2395→ 1062	106202
TL or CA/AT	08
TL or CA/AT	00
*(See Note "Sum check data")	

(2) Next, push every key on the keyboard except for the receipt and journal keys.
When the [TL] or [CA/AT] key is depressed, the termination printout is immediately produced assuming that all keys have been depressed.
There is no order in which the keys have to be depressed.

[Keyboard position code of model vs. key to be depressed]
[All key position code]

		20	21		37	34		44	46
↑	↑	25	24	27	36	38		45	47
48	40	6	7	8	39	35		41	49
18	15	3	4	5	30	32		43	42
14	13	0	1	2	29	33		23	17
11	12	10	26	9	28	31		22	16

Fig. 7-1

[ER-1910]

		X	X		37		X	X
↑	↑	25	24	27	X	X	45	
48	40	6	7	8			41	
18	15	3	4	5		32	43	
14	13	0	1	2				17
11	12	10		9		31	TL	

Fig. 7-2

[ER-1920]

		20			37		44	46
↑	↑	25	24	27	36	38	45	47
48	40	6	7	8	39	35	41	
18	15	3	4	5	30	32	43	
14	13	0	1	2		33		17
11	12	10		9		31	TL	

Fig. 7-3

[ER-2385]

		20	21		37	34	44	
↑	↑	25	24	27		38	45	
48	40	6	7	8		35	41	
18	15	3	4	5		32	43	42
14	13	0	1	2		33		17
11	12	10		9		31	CA/AT	

Fig. 7-4

[ER-2395]

		20	21		37	34	44	46
↑	↑	25	24	27	36	38	45	47
48	40	6	7	8	39	35	41	49
18	15	3	4	5	30	32	43	42
14	13	0	1	2		33		17
11	12	10		9		31	CA/AT	

Fig. 7-5

② Description
Until the depression of the [TL] or [CA/AT] key, the sum of key position codes is compared with the sum check data, except for the [TL] or [CA/AT] key.

③ Termination
The test terminates with the depression of the [TL] or [CA/AT] key and the termination printout is produced.

Termination printout 02

Termination printout with error -------02E

NOTE: Sum check data
The sum check data shown in the example is based on the standard key layout for the each model.
If the machine has a key layout other than the standard layout, the sum check must be calculated by adding all the key position codes to be depressed, then use the sum as its sum check data. (Refer to Fig. 7-1)

3) Test No.3: Display buzzer test
① Key operation

3 → [TL] or [CA/AT]

② Description
Continuous beeps and display are tested.

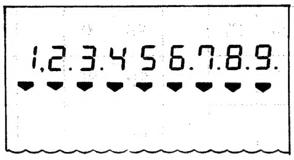


Fig. 7-6

③ Termination
The beep stops with any key depression and the display returns to show 0.
Termination print 03

4) Test No.4: Receipt on/off switch test
① Key operation

4 → [TL] or [CA/AT]

② Description
The following is displayed according to the location of the receipt on/off switch.

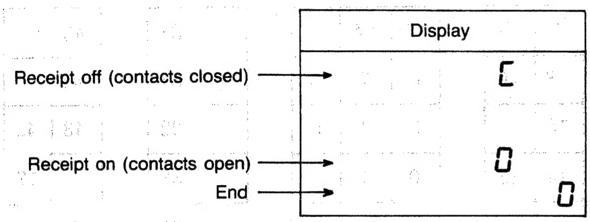


Fig. 7-7

③ Termination
With depression of any key, the display shows 0.
Termination print 04

5) Test No.5: Drawer open test
① Key operation

5 → [TL] or [CA/AT]

② Description
With this test, the drawer opens and its state is displayed in the following manner:
Drawer open → O
Drawer closed → C
"C" is displayed for the model that has no drawer sensor switch.
③ Termination
With depression of any key, the display shows 0.
Termination print 05

6) Test No.6: Continuous print test
① Key operation

9 → [TL] or [CA/AT]

② Description
Receipt switch at OFF: Continuous printing is done.
Receipt switch at ON: After a cycle of printing, the operation terminates automatically.
③ Termination
When the receipt switch is turned from OFF to ON position while printing is continuing, the test termination after a cycle of printing.

[A continuous print example]

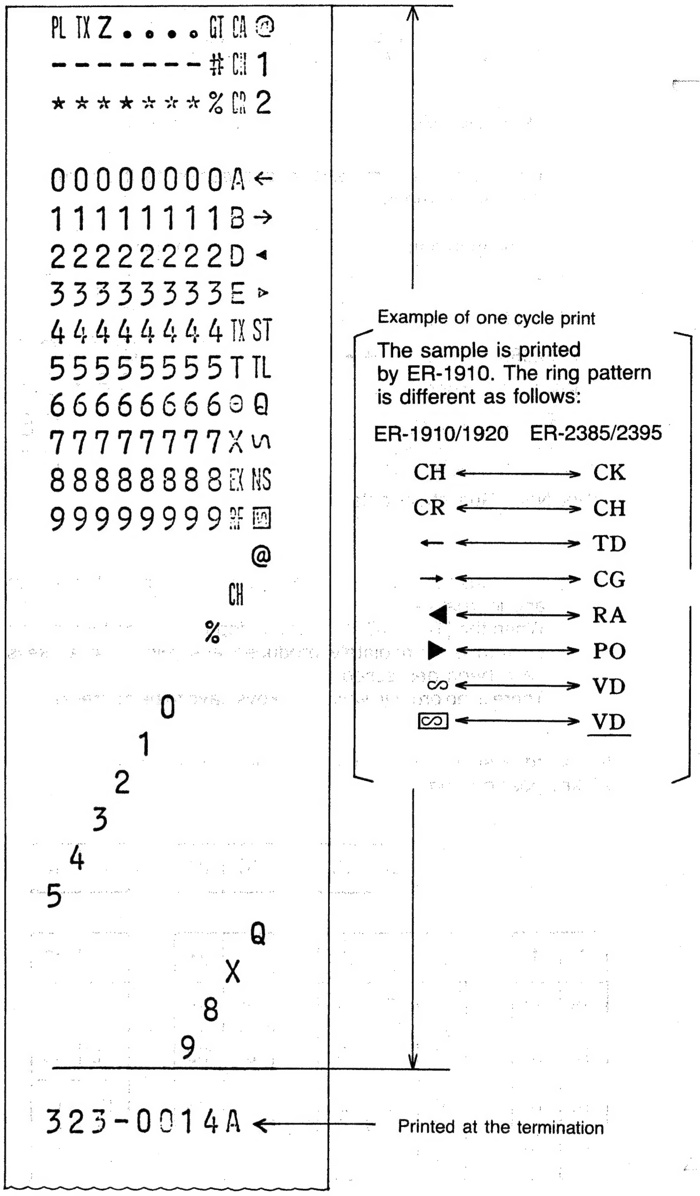


Fig. 7-8

7) Test No.7: ROM test
① Key operation
CPU internal system ROM (0000H~0FFFH)

10 → [TL] or [CA/AT]

CPU internal application ROM (8000H~FF7FH) or 27256 SOS ROM

11 → [TL] or [CA/AT]

27128/SOS ROM (2000H~3FFFH)

12 → [TL] or [CA/AT]

② Test results
Termination print

Normal end	At error
1 0	– – – – – – 1 0 E
1 1	– – – – – – 1 1 E
1 2	– – – – – – 1 2 E

8) Test No.8: RAM test

① Key operation

13 → [TL] or [CA/AT]

② Description

Though read/write test is conducted from the address 4000H to 5FFFH, the data are secured as they are saved before the test started.

③ Test results Termination print

At normal end → 1 3

Error → 1 3 E

9) Test No.9: Key position code read test

① Key operation

14 → [TL] or [CA/AT]

② Description

Key position of a key on the keyboard is displayed when any key is depressed. (Hardware key contacts code)
The receipt and journal keys only feed paper without displaying, and the [TL] or [CA/AT] key is used to terminate the test.
For key position codes displayed, refer to Fig.7-1 to 7-5.

③ Termination

Push the [TL] or [CA/AT] key.
Termination print 14

10) Test No.10: System clock test

① Key operation

15 → [TL] or [CA/AT]

② Description

Used for the adjustment of the KDC (μPD7505C) system clock.
An 880 to 900μs pulse is generated from P21 (pin 30) of the KDC. The display becomes blanking.
For detail of adjustment, refer to the paragraph discussing circuit description.

③ Termination

Set the mode switch to the PGM side.
Termination print 15

11) Test No.11: Counter clock test

① Key operation

16 → [TL] or [CA/AT]

② Description

For error adjustment, a 2048Hz pulse is issued from P21 (pin 3) of the KDC (μPD7507C). The display goes blank.
This test is for the factory adjustment only.

③ Termination

Set the mode switch to the PGM side.
Termination print 16

12) Test No.12: Sequential test-1

① Key operation

x x x x 00 → [TL] or [CA/AT]

Refer to 2) test No.2 for the sum check data.

② Description

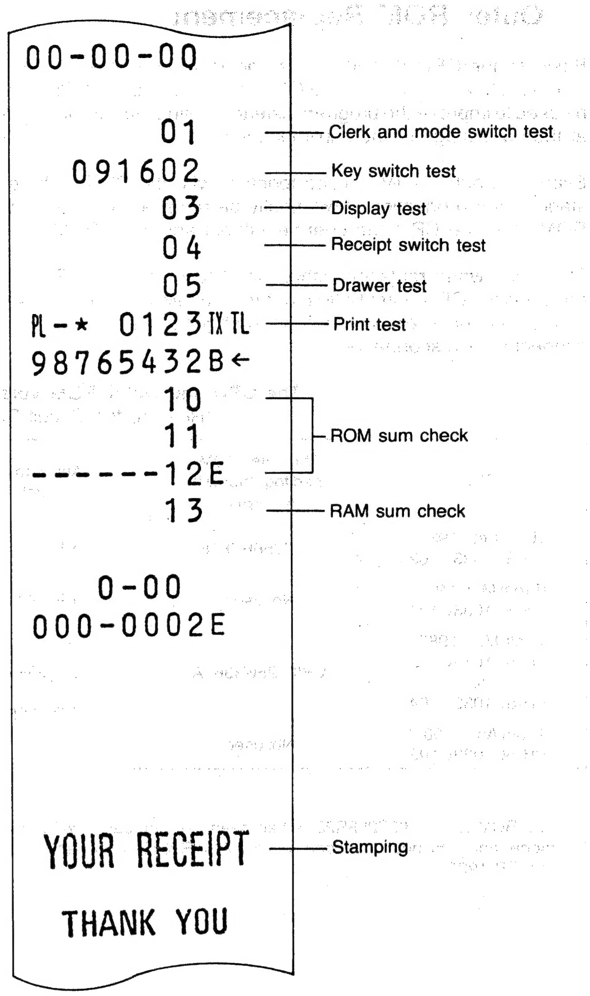
Within one second after the key operation, the test nos 1 thru 8, are able to carry out continuously.

NOTE-1: If a drawer sensor is equipped for test NO.5, the control proceeds to a next step when the drawer is closed after it was opened. If the sensor is not equipped, the control jumps to a next step assuming it has no drawer is installed.

NOTE-2: Simple print is done for the continuous print test of test No.6.

NOTE-3: An error is always evoked, if the 27128 SOS ROM is not mounted or 27256 SOS ROM is mounted at test No.7-12.

[A print example after the test]



* The upper four digits shows the sum of key position codes which have been pressed in the key switch test.

Fig. 7-9

③ Termination

All tests automatically terminate upon finishing the stamp test.

13) Test No.13: Sequential test-2

① Key operation

x x x x 22 → [TL] or [CA/AT]

Refer to 2) test No.2 for the sum check data.

② Description

It is similar as the test No.12 except that it ignores the drawer open sensor of the test No.5.

8. Service Precaution on the CPU and Outer ROM Replacement

Basically the CPU SC1003C is so designed to operate by its own program stored in the internal ROM. However, an outer ROM may be used to improve the program instead of using the internal ROM at the early stage of the implimentation.

Even if an outer ROM is used together with the CPU at the early stage of the production, it will finally be replaced with the internal ROM, then the CPU can operate without any outer ROM.

Therefore, when replacing either the CPU or the outer ROM, or replacing the CPU/outer ROM together to a new CPU, the following care should be exercised and the each jumper wire must be connected or disconnected.

The CPU and Outer ROM Version and the Jumper Wire Connection Table
(Refer to the Circuit Diagram 00ZER2395CD1M on page 5)

CPU	The outer ROM used together with the CPU.	Applicable models	Jumper wires	J1		J2		J3		J4
			Terminal Name (Signal)	C-1 (+5V)	C-2 (A15)	C-1 (+5V)	C-2 (A14)	C-1 (A15)	C-2 (CS2)	(GND)
(Until Feb. 1987) VHISC1033C102	VHI27256R281B*1	ER-1910	Jumper wire connection	X	O	X	X	O	X	O
(From Mar. 1987) VHISC1033C104	Not used	ER-1920		X	O	X	X	X	X	Δ
(Until Mar. 1987) VHISC1033C102 or VHISC1033C104	VHI27256R361A	ER-2385		O	X	X	O	O	X	O
(From April. 1987) VHISC1033C103	Not used	ER-2395		X	O	X	X	X	X	Δ

O : To be connected.
X : To be disconnected.
Δ : When J4 is being connected, it may leave as it is.

*1: The ROM type VHI27256R281A had been used for Jan. 1987 production except for Switzerland model and has been changed to VHI27256R281B from Feb. 1987 production for all ER-1910 and ER-1920.